REMARKS

The Examiner is thanked for the thorough examination of the present application. However, the Office Action has continued to reject all claims 1-16. Specifically, the Office Action has rejected claims 1-15 as allegedly unpatentable over the combination of U.S. Patent No. 6,801, 202 to Nelson in view of U.S. Patent No. 6,311,247 to Spencer. Further, the Office Action has rejected claim 16 under 35 U.S.C. § 103(a) as allegedly unpatentable over Nelson and Spencer in further view of U.S. Patent No. 6,924,807 to Ebihara. Applicants have made a cosmetic amendment to claim 7. For at least the reasons set forth herein, Applicants respectfully disagree with the rejections and request that the rejections be withdrawn.

Before addressing the substantive rejections, Applicants first address the objection that has now been raised to the drawings. Although the initial examination and first Office Action mailed in this application raised no objections to the drawings, the present Office Action objects to the drawings as failing to show the "partitioning logic" of claims 7 and 10-11. Applicants respectfully submit that the drawings, as filed, are in full compliance with all relevant statutes and regulations. The Office Action has objected to the drawings under 37 C.F.R. § 1.83(a), stating that every feature of the claimed invention must be separately illustrated in the drawings. However, 37 C.F.R. §1.83(a) provides that the drawing illustrations may consist of, for example, a labeled rectangular box, where a "detailed illustration is not essential for a proper understanding of the invention." Referencing the drawings that were filed in this application, both Figures 3 and 4 illustrate a block labeled as "Chip Set" 218, and the function of the partition logic within the chip set 218 is described in the specification. Further, Fig. 5 includes a specific block labeled "partitioning state-sequenced information" 402.

Accordingly, Applicants respectfully submit that these drawings are sufficient to fully comply with all statutory and regulatory requirements. Moreover, if any drawing amendments were to be made, Applicants would simply submit a drawing amendment to Fig. 3 or 4 adding a block labeled as "partition logic" as forming a part of the "Chip Set" 218. In view of the existing description of the specification, as well as the drawing of Fig. 5, the undersigned respectfully submits that such a drawing amendment would add nothing to the content of the present application. For at least these reasons, the drawing objection should be withdrawn.

Turning now to the substantive rejections of the claims, the Office Action has rejected claims 1-15 under 35 U.S.C. § 103(a) as allegedly obvious over the combination of Nelson in view of Spencer. For at least the reasons set forth below, the undersigned respectfully traverses this application of the cited art against the presently pending claims. With regard to the application of the Spencer patent, the undersigned notes that the Spencer patent is assigned to the assignee of the present invention. More significantly, the undersigned attorney is the attorney who drafted and prosecuted the Spencer patent, and for this reason is particularly knowledgeable as to the specific teachings of this patent (or lack thereof, in the context of the present application).

The Office Action alleged that:

> Spencer teaches a computer system (Fig. 2) comprising a host processor (112) configured to execute a single-threaded application; partitioning logic (123) for partitioning the state-sequenced information, communication logic (chipset 120) configured to communication partitioned state-sequenced information across a plurality of I/O busses (PCI buses 116-118); a plurality of interfaces (124-128) located at a subsystem for receiving the information communication across the plurality of I/O busses; processing logic (not shown, but would have been obvious to connect any peripheral (I/O) devices into the PCI busses 116-118, for example, graphics processor is considered one of the peripheral device) for controlling the

processing of the partitioned information without re-sequencing the information, the processing logic configured to preserve state information of the information processed.

This is, in fact, not what Spencer teaches. Instead, Spencer is directed to a system and method for interfacing a system bus to a plurality of PCI busses. As is described in Spencer, previous systems interfaced with external PCI devices via a shared PCI bus. The system of Spencer provided multiple PCI busses, which were dedicated to different devices and allowed communications to each device to take place over a dedicated PCI bus. Figure 4 of the Spencer reference illustrates an embodiment of an architecture for interfacing a system bus with such multiple PCI busses or PCI bus interfaces.

Returning to the application of Spencer (quoted above) made by the Office Action, the Office Action stated that "Spencer teaches...a host processor (112) configured to execute a single-threaded application; partitioning logic (123) for partitioning the state-sequenced information..." First, there is no teaching in Spencer of the host processor being "configured to execute a singe-threaded application." As noted above, and as is specifically taught in Spencer, the embodiments described therein relate to the interfacing of a system bus interface with multiple PCI bus interfaces. The application being executed on the host processor could be a single-threaded application, or could be a multi-threaded application (Spencer is simply silent on this point, as it is not a feature germane to that disclosure). More significantly, the Office Action alleged that Spencer discloses "partitioning logic (123) for partitioning state-sequenced information..." Reference numeral 123 of Spencer is illustrated in Figure 4 and broadly denotes an architecture of an embodiment of an I/O controller (see column 5, line 15). The function of this architecture is to interface the system bus interface with multiple PCI bus interfaces for both incoming and outgoing PCI communications. Significantly, there is absolutely no teaching or suggestion in Spencer relating to the partitioning of state-

sequenced information, as this is not a feature that is germane to the disclosure of Spencer. For at least this reason, the Office Action's application of Spencer to the embodiments of the invention that are defined in each of the independent claims is misplaced.

In this regard, independent claims 1 and 7 recite:

> 1. A method comprising:
> ***partitioning state-sequenced information for communication to a computer subsystem;***
> communicating the partitioned information to the subsystem over a plurality of input/output busses; and
> ***separately processing partitioned information received over each of the plurality of input/output busses, without first re-sequencing the information.***
>
> 7. A computer system comprising:
> a host processor configured to execute a single-threaded application;
> ***partitioning logic for partitioning state-sequenced information,***
> communication logic configured to communicate partitioned state-sequenced information across a plurality of input/output busses;
> a plurality of interfaces located at a subsystem for receiving the information communicated across the plurality of the input/output busses;
> ***processing logic for controlling the processing of the partitioned information without re-sequencing the information, the processing logic configured to preserve state information of the information processed.***

(*Emphasis added.*) As emphasized above, Independent claim 1 includes, among other features, "partitioning state-sequenced information for communication to a computer subsystem." Likewise, claim 7 defines "partitioning logic for partitioning state-sequenced information." There is simply no disclosure or suggestion in Spencer (as alleged by the Office Action) of this claimed feature. For at least this reason, the rejections of independent claims 1 and 7 are misplaced and should be withdrawn. For at least the same reasons, all remaining claims 2-6 and 8-16, which depend from independent claims 1 and 7, respectfully, should be withdrawn as well.

Further, with regard to independent claim 7, this claim recites "processing logic for controlling the processing of the partitioned information without re-sequencing the information, the processing logic configured to preserve state information of the information processed." On page 4, lines 7-9 of the Office Action, the Office Action admits that this processing logic is not shown in Spencer, but instead alleges that it would have been obvious. Applicants respectfully disagree. In fact, the reason that such logic is neither illustrated nor suggested in Spencer is that such logic would be completely counter to the objective of the invention of Spencer. As noted above, Spencer is directed to a system and method for interfacing a system bus interface with multiple PCI bus interfaces. In doing so, a host computer can communicate directly, over dedicated PCI busses, to multiple devices that communicate via a PCI bus. Even assuming, for the sake of argument, that Spencer showed the partitioning of state-sequenced information and the communication of that information over the independent PCI busses to multiple PCI devices, each such device would thereafter perform its operations independently of the other PCI devices and therefore would have no reason or need to re-sequence any state-sequenced information. Indeed, the fact that the PCI devices are devices that operate independently underscores the fact that the information being sent to these devices independently does not originate from state-sequenced information.

For example, and as disclosed in Spencer, examples of PCI devices include "disc drive controllers, video cards, modems or other communication devices, etc." (Spencer, column 6, lines 27-28). The undersigned respectfully submits that a person skilled in the art would recognize that information sent to a disc drive controller, would not be linked, in a state-sequenced fashion, with information sent to devices like video cards, modems, etc. Accordingly, a person skilled in the art would not construe the teachings of Spencer to include, implicitly or inherently, either logic to partition state-sequenced information for

communication over PCI busses or logic configured to process the partitioned information while preserving state information of the information processed (as alleged by the Office Action). For at least this additional reason, the rejection of independent claims 7 (as well as dependent claims 8-16) is misplaced and should be withdrawn.

Similarly, the feature of dependent claim 2 calls for "obtaining state information from the received information, and processing the information in a proper state context." The Office Action has not even alleged, with specificity, that this claimed feature is taught in any of the cited art. In this regard, in rejecting claim 2, the Office Action merely stated that "claims 1, 2, and 4-6 are similar in scope to system claims 7-15 above and thus are rejected under similar rationale." (Office Action, page 5, lines 9-10). However, the feature just quoted from claim 2 is not referenced anywhere in the Office Action's rejection of claim 7. Accordingly, and for at least this additional reason, the rejection of claim 2 is misplaced and should be withdrawn.

As a separate and independent basis for the patentability of all claims, the undersigned further submits that the Office Action's application of the Nelson reference is similarly misplaced. In this regard, the system of Nelson is directed to a graphics system that is configured to perform parallel processing of graphics data using multiple graphics pipelines. Significantly, rather than partitioning [graphics] information for communication over multiple I/O busses, as required by the claims of the present invention, Nelson merely describes the division of graphics information into a plurality of "rendering units" (reference numbers 150A-150D). In fact, Fig. 3 of Nelson illustrates a control unit 140 that interfaces to a computer system via a single high-speed bus (not multiple I/O busses). Once the information is received by the control unit 140, it is split among a plurality of rendering units for processing. This parallel processing is simply inapplicable to the features of the claimed

invention, which call for the partitioning of state-sequenced information for communication over a plurality of I/O busses, and the subsequent processing of the state-sequencing information without first re-sequencing the data. As noted above, the alleged teachings of Spencer for allegedly disclosing the multiple I/O busses and the processing of state-sequenced information is misplaced. For at least this separate and independent reason, the rejection of independent claims 1 and 7 are misplaced and should be withdrawn.

As a separate and independent basis for the patentability of these claims, Applicants respectfully submit that the Office Action has failed to cite a proper suggestion or motivation for combining Spencer with Nelson. In combining these references, the Office Action stated only that the combination would have been obvious "because multiple separate busses allows exclusive communication by providing a direct pipe therebetween and thus provides significant performance enhancements over prior art systems that have shared PCI busses as taught by Spencer (abstract)." First, this cited teaching from Spencer refers to the advantage of providing dedicated PDI busses between a device and multiple devices that intercommunicate with the device over PCI busses. However, it does NOT suggest the modification of the parallel processing pipelined architecture of Nelson to have multiple I/O busses.

Further, the alleged motivation is clearly improper in view of well-established Federal Circuit precedent. It is well-settled law that in order to properly support an obviousness rejection under 35 U.S.C. § 103, there must have been some teaching in the prior art to suggest to one skilled in the art that the claimed invention would have been obvious. W. L. Gore & Associates, Inc. v. Garlock Thomas, Inc., 721 F.2d 1540, 1551 (Fed. Cir. 1983). More significantly,

> "The consistent criteria for determination of obviousness is whether the prior art would have suggested to one of ordinary skill in the art that this [invention] should be carried out and would have a reasonable likelihood of success, viewed in light of the prior art. ..." Both the suggestion and the expectation of success must be founded in the prior art, not in the applicant's disclosure... In determining whether such a suggestion can fairly be gleaned from the prior art, the full field of the invention must be considered; for the person of ordinary skill in the art is charged with knowledge of the entire body of technological literature, including that which might lead away from the claimed invention."

(*Emphasis added.*) In re Dow Chemical Company, 837 F.2d 469, 473 (Fed. Cir. 1988).

In this regard, Applicants note that there must not only be a suggestion to combine the functional or operational aspects of the combined references, but that the Federal Circuit also requires the prior art to suggest both the combination of elements and the structure resulting from the combination. Stiftung v. Renishaw PLC, 945 Fed.2d 1173 (Fed. Cir. 1991). Therefore, in order to sustain an obviousness rejection based upon a combination of any two or more prior art references, the prior art must properly suggest the desirability of combining the particular elements to derive a system and method for communicating state-sequenced information over multiple I/O busses, as claimed by the Applicants.

When an obviousness determination is based on multiple prior art references, there must be a showing of some "teaching, suggestion, or reason" to combine the references. Gambro Lundia AB v. Baxter Healthcare Corp., 110 F.3d 1573, 1579, 42 USPQ2d 1378, 1383 (Fed. Cir. 1997) (also noting that the "absence of such a suggestion to combine is dispositive in an obviousness determination").

Evidence of a suggestion, teaching, or motivation to combine prior art references may flow, inter alia, from the references themselves, the knowledge of one of ordinary skill in the art, or from the nature of the problem to be solved. See In re Dembiczak, 175 F.3d 994, 1000, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Although a reference need not expressly teach that the disclosure contained therein should be combined with another, the showing of

combinability, in whatever form, must nevertheless be "clear and particular." Dembiczak, 175 F.3d at 999, 50 USPQ2d at 1617.

If there was no motivation or suggestion to combine selective teachings from multiple prior art references, one of ordinary skill in the art would not have viewed the present invention as obvious. See In re Dance, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998); Gambro Lundia AB, 110 F.3d at 1579, 42 USPQ2d at 1383 ("The absence of such a suggestion to combine is dispositive in an obviousness determination.").

Significantly, where there is no apparent disadvantage present in a particular prior art reference, then generally there can be no motivation to combine the teaching of another reference with the particular prior art reference. Winner Int'l Royalty Corp. v. Wang, No 98-1553 (Fed. Cir. January 27, 2000).

For at least the additional reason that the Office Action failed to identify proper motivations or suggestions for combining the various references to properly support the rejections under 35 U.S.C. § 103, the rejections of claims 1-15 should be withdrawn. Similarly, the rejection of claim 16 should be withdrawn, as it has been rejected on even the more tenuous combination of Nelson and Spencer in further view of Ebihara. The Office Action alleged that this further combination would have been obvious "in order to provide synchronization among multiple graphics processors and thus to provide synchronized output signals." (Office Action, p. 6, lines 6-8). Applicants submit that this rationale is inconsistent with the relevant legal precedent set out above, and request that the rejection of claim 16 be withdrawn.

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CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this Amendment and Response to Office Action. If, however, any fee is deemed to be payable, you are hereby authorized to charge any such fee to Hewlett-Packard Company's Deposit Account No. 08-2025.

Respectfully submitted,

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